

**TURBO-XT
Main Board
Installation Guide**

2012

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CHAPTER 1 INTRODUCTION

1-1 General

The TURBO—XT is an Intel 8088-2 microprocessor-based system. It can run the most popular software packages like WORDSTAR, DBASEII, LOTUS 1-2-3, AUTOCAD, SYMPHONY and so on. But please note use Normal mode (4.77 MHz) When running copy WRITE.

The following manual will provide detailed functions and using for TURBO—XT.

1-2 Description

The TURBO—XT system board fits horizontally in the base of the system unit and is approximately 8 1/2 12 inches. It is two layer P.C.B. DC power and a signal from the power supply enter the board through 12 pin connectors. Other connectors on the board are for attaching the keyboard and speaker. Eight 62-pin card edge-sockets are also mounted on the board. The I/O channel is bussed across these eight I/O slots.

A dual-in-line package (DIP) switch (SWI) (one eightswitch

pack) is mounted on the board and can be read under program control. The DIP switch provides the system software with information about the installed options, how much storage the system board has, what type of the display adapter is installed, what operation modes are desired when power is switched on (color or black-and-white, 80-or 40-character lines), and the number of diskette drive attached.

The system board consists of five functional area: the processor subsystem and its support elements, the read-only memory (ROM) subsystem, the read/write (R/W) memory subsystem, integrated I/O adapters, and the I/O channel. All are described in this section.

The heart of the TURBO-XT system board is the Intel 8088-2 micro-processor. This processor is an 8-bit external bus version of Intel's 16-bit 8086 processor, and is software-compatible with the 8086. Thus, the 8088-2 supports 16-bit operations, including multiply and divide. It also operates in maximum mode, so a coprocessor can be added as a feature. In normal mode. The processor operates at 4.77 MHz. This frequency, which is derived from a 14.318 MHz crystal. When you change mode to turbo mode. Will give you an increase of almost 70% in speed of program execution. At the time, the processor operates at 8MHz.

The processor is supported by a set of high-function support

devices providing four channels of 20-bit direct-memory access (DMA), three 16-bit timer-counter channels, and eight prioritized interrupt levels.

Three of the four DMA channels are available on the I/O bus and support high speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programming a channel of the timer-counter device to periodically request a dummy DMA transfer. This action creates a memory-read cycle, which is available to refresh dynamic storage both on the system board and in the system expansion slots.

The three programmable timer/counters are used by the system as follows: Channel 0 is used as a general-purpose timer providing a constant time base for implementing a time-of-day clock; Channel 1 is used to time and request refresh cycles from the DMA channel; and Channel 2 is used to support the tone generation for the audio speaker.

Of the eight prioritized levels of interrupt, six are bussed to the system expansion slots for use by features cards. Two levels are used on the system board. Level 0, the highest priority, is attached to Channel 0 of the timer/counter and provides a periodic interrupt for the time-of-day clock. Level 1 is attached to the keyboard adapter circuits and receives an interrupt of each scan

code sent by the keyboard. The non-maskable interrupt (NMI) of the 8088-2 is used to report memory parity errors.

The system board supports both ROM/EPROM and R/W memory. It has space for 64K x 8 of ROM or EPROM. This ROM contains the power-on self-test, I/O drivers, dot patterns for 128 characters in graphics mode, and It also has of 64K R/W memory. Memory greater than the system board has a maximum of all R/W memery is parity checked.

The system board contains the adapter circuits for attaching the serial interface from the keyboard. These circuits generate an interrupt to the processor when a complete scan code is received. The interface can request execution of a diagnostic test in the keyboard.

The keyboard interface is a 5-pin DIN connector on the system board that extends through the rear panel of the system unit.

The system units has an 2-1/4 inch audio speaker. The speaker's control circuits and driver are on the system board. The speaker connects through a 2-wire interface that attaches to a 3-pin connector on the system board.

The speaker drive circuit is capable of approximately 1/2 watt

of power. The control circuits allow the speaker to be driven three different way: 1) a direct program control register bit may be toggled to generate a pulse train; 2) the output from Channel 2 of the timer counter may be programmed to generate a waveform to to speaker; 3) the clock input to the timer counter can be modulated with a program-controlled I/O register bit. All three methods may be performed simultaneously.

The TURBO-XT has the following components

- * Intel 8088-2 microprocessor.
- * Socket for 8087-2 math co-processor.
- * Either a 256 KB or a 640 KB random-access memory (RAM) subsystem.
- * Running at 4.77 MHz (8 MHa option).
- * 8 input/ouput (I/O) slots with 62-pins card-edge socket.
- * Disk Storage:
 - Base Model: two 5-1/4" floppy disk drive with 360 KB.
 - Enhanced Model: can add one 20 MB Harddisk drive.

1-3 I/O Channel

The I/O channel is an extension of the 8088-2 microprocessor bus. It is, however, demultiplexed, repowered, and enhance by the addition of interrupts and direct memory access (DMA) functions.

The I/O channel contains an 8 bit, bidirectional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines, a channel check line, and power and ground for the adapters.

I/O devices are addressed using I/O mapped address space. The channel is designed so that 768 I/O device addressed are available to the I/O channel cards.

A channel check line exists for reporting error conditions to the processor. Activating this line results in a Non-Maskable Interrupt (NMI) to the 8088-2 processor. Memory expansion options use this line to report parity errors.

1-4 I/O Channel Description

The following is a description of the I/O Channel. All lines are TTL-compatible.

Singal I/O Description:

OSC, Oscillator:

High speed clock with a 70-ns period (14.31818 MHz). it has a 50% duty cycle.

CLK, System Clock:

It is divide-by-three of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.

RESET:

This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.

A0-A19, Address Bits 0 to 19:

These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the Least Significant Bit (LSB) and A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.

D0-D7, I/O Data Bits 0 to 7:

These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These lines are active high.

ALE, Address Latch Enable:

This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched

with the falling edge of ALE.

I/O CH CK, I/O Channel Check:

This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error would be indicated.

I/O CH RDY, I/O Channel Ready:

This line, normally high (ready), can be pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low, longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).

IRQ2-IRQ7, Interrupt Request 2 to 7:

These lines are used to signal the processor, that a I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high, until it was acknowledged by the processor (interrupt service routine).

IOR, I/O Read Command:

This command line instructs an I/O device to drive its data

into the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

LOW, I/O Write Command:

The command line instructs an I/O device, to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMR, Memory Read Command:

This command line instructs the memory to drive its data into the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMW, Memory Write Command:

This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

DRQ1-DRQ3, DMA Request 1 to 3:

These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK line goes active.

DACK0–3—DMA Acknowledge 0 to 3:

These lines are DACK3 used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active low.

AEN, Address Enable:

This line is used to degate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).

T/C, Terminal Count:

This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

CHAPTER 2 SETTING TURBO—XT

The DIP Switch (SWI) is used to set the system configuration and specify the amount of memory installed on the mainboard.

2-1 The System Board Switch Setting:

POSITION	FUNCTION
1,	Normal operation off
2	Use for 8087-2 Math Coprocessor
3,4	Amount of memory on system board.
5,6	Type(s) of display(s) connected
7,8	5-¼" diskeette drives installed

Math Coprocessor

(SWI)	FUNCTION
2—OFF	(Normal operation)
2—ON	W/O 8087-2 Coprocessor
2—OFF	W/ 8087-2 Coprocessor

Memory Switch Settings.

3=OFF	4=ON	128K INSTALLED
3=ON	4=OFF	192K INSTALLED
3=OFF	4=OFF	256K INSTALLED

Type(s) of Display(s) Connected

Type of Display	(SW1)	
(None)	5-ON	6-ON
Monochrome Display	5-OFF	6-OFF
Color Display (40*25 MODE)	5-OFF	6-ON
Color Display (80*25 MODE)	5-ON	6-OFF







Number of 5-¼" Diskette Drives Installed

Number	Switch 1	
1-Drives	7-ON	8-ON
2-Drives	7-OFF	8-ON
3-Drives	7-ON	8-OFF
4-Drives	7-OFF	8-OFF

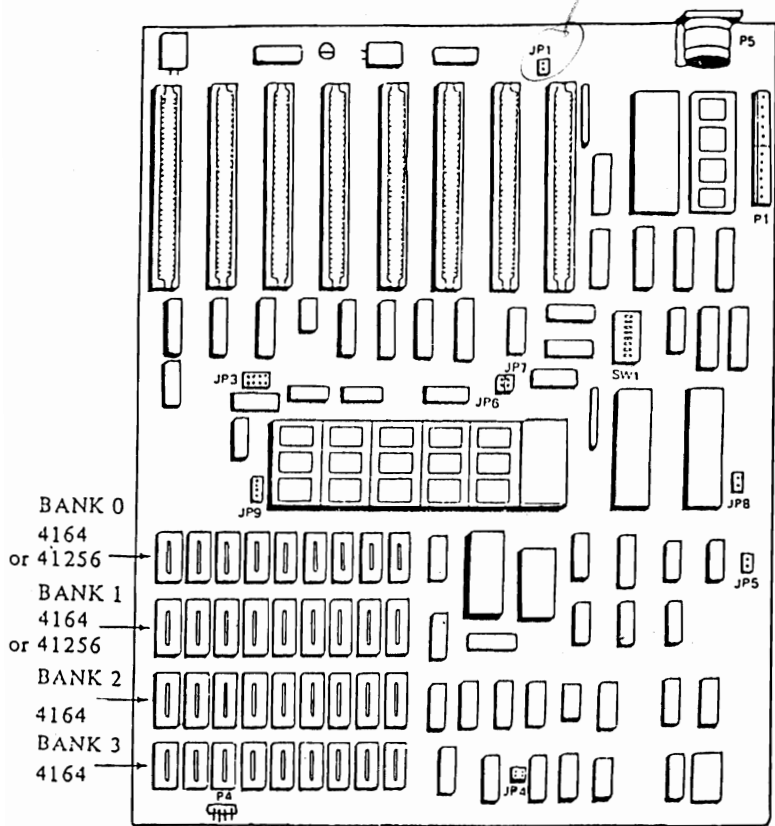
2-2 How to Change the System Board Memory (256KB/640KB)

1. If you want set TURBO-XT on 256KB then.
You must plug RAM Bank 0,1,2,3 full with 64K Dynamic 4164 chips. or plug RAM Bank 0 full with 256K Dynamic 41256 chips. And set JP3 and JP4 as indicated below table.
2. If you want set TURBO-XT on 640 KB then.
You must plug RAM bank 0,1 full with 256K Dynamic 41256 RAM chip. And plug bank 2,3 full with 64K Dynamic 4164

chips. And set JP3, JP4 as following table.

Option	BANK 0	BANK 1	BANK 2	BANK 3	Jumper Location	
					JP3	JP4
256K	4164x9	4164x9	4164x9	4164x9		
256K	41256x9	none	none	none		
512K	41256x9	41256x9	none	none		
640K	41256x9	41256x9	4164x9	4164x9		

— The TURBO—XT diagram —



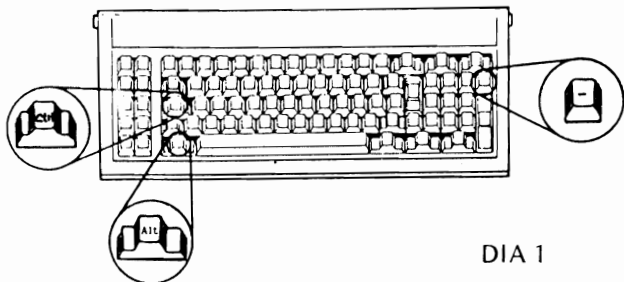
CHAPTER 3 HOW TO USE THE TURBO—XT SYSTEM

The TURBO—XT Supports both software switch as well as hardware switch to allow transaction from Normal mode to Turbo mode vice versa.

3-1 SOFTWARE SWITCH (with ERSO/DTK TURBO BIOS or modified BIOS For TURBO Use)

please set Jumper (JP7) "ON" For software switch. and then following procedure.

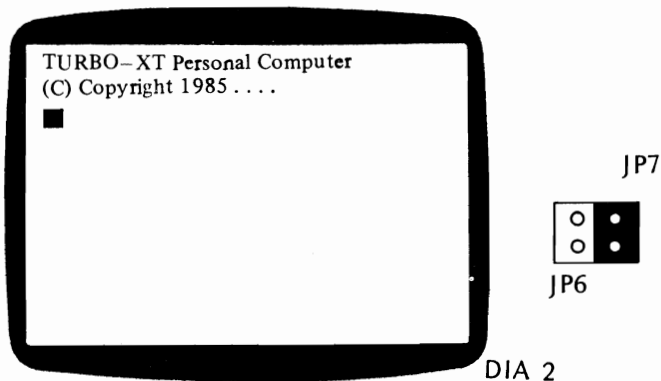
- 1) Press and hold "Ctrl." and "Alt" keys.
- 2) Press the "-" key on the numeric keyboard see dia 1.



DIA 1

The TURBO-XT will give you an increase of almost 70% in speed of program execution.

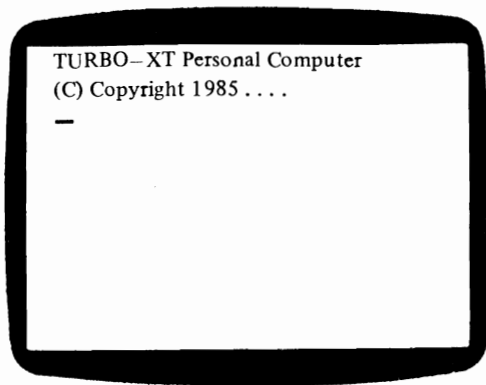
After transition to the turbo mode the cursor will appear as a "box" see dia 2.



Returning from "Turbo" to "Normal" mode
Procedure:

- 1) Press and hold "Ctrl" and "Alt" keys.
- 2) Press the "-" key on the numeric keyboard.

After returning to the normal mode the cursor will again appear as a "dash".

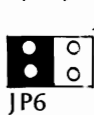


DIA 3

N.b. On returning to the normal mode a character code may appear on the screen Cancel it or press "Return".

3-2 HARDWARE SWITCH

Set Jumper JP6 "ON" For hardware switch



- 1) Turn on Turbo mode:
In "ON" position to turn on Turbo mode at 8MHz.
- 2) Return to Normal mode:

Push to Turbo switch into “OFF” position to come back to Normal mode at 4.77 MHz.

The push button leads to JP5 on mainboard, the push button at “ON” position that means shorted circuit on the 2pins of JP5, At “OFF” position. When the circuit is open.

—APPENDIX—

The system board has the following connectors:

- Speaker connector (P4)
- Two power-supply connectors (P1) and (P2)
- Keyboard connector (P5)
- Power LED and TURBO LED connector (JP9)
- Turbo control connector (JP5, JP6, JP7)
- Keylock connector (JP8)
- 256K/512K/640K memory select (JP3, JP4)

The speaker connector is a 4-pin, keyed 90 degree. The pin assignments follow.

Pin	Function
1	Data out
2	35 Vdc
3	Ground
4	+5 Vdc

connect pin 1 &
pin 2 to speaker,
or pin 1 & pin 4
to speaker

Speaker Connector (P4)

The pin assignments for power-supply connectors, P1 and P2 are as follows:

Pin	Assignments	Connector
1	Power good	P1
2	Not used	
3	+12 Vdc	
4	-12 Vde	
5	Ground	
6	Ground	
1	Ground	P2
2	Ground	
3	-5 Vdc	
4	+5 Vdc	
5	+5 Vdc	
6	+5 Vdc	

Power Supply connectors

The keyboard connector is a 5-pin, 90-degree Printed Circuit Board (PCB) mounting, DIN connector. The pin assignments are as follows:

Pin	Assignments
1	Keyboard clock
2	Keyboard data
3	Keyboard reset
4	Ground
5	+5 Vdc

Keyboard Connector (P5)

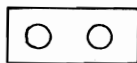
The power LED and LED connector is a 4-pin Berg strip. Its pin assignments follow:

Pin	Assignments
1	Turbo LED (1)
2	Tubo LED (2)
3	LED POWER
4	Ground

pin 1 & pin 2 connector to turbo
LED pin 3 & pin 4 to power on LED

Power LED and Keylock Connector (JP9)

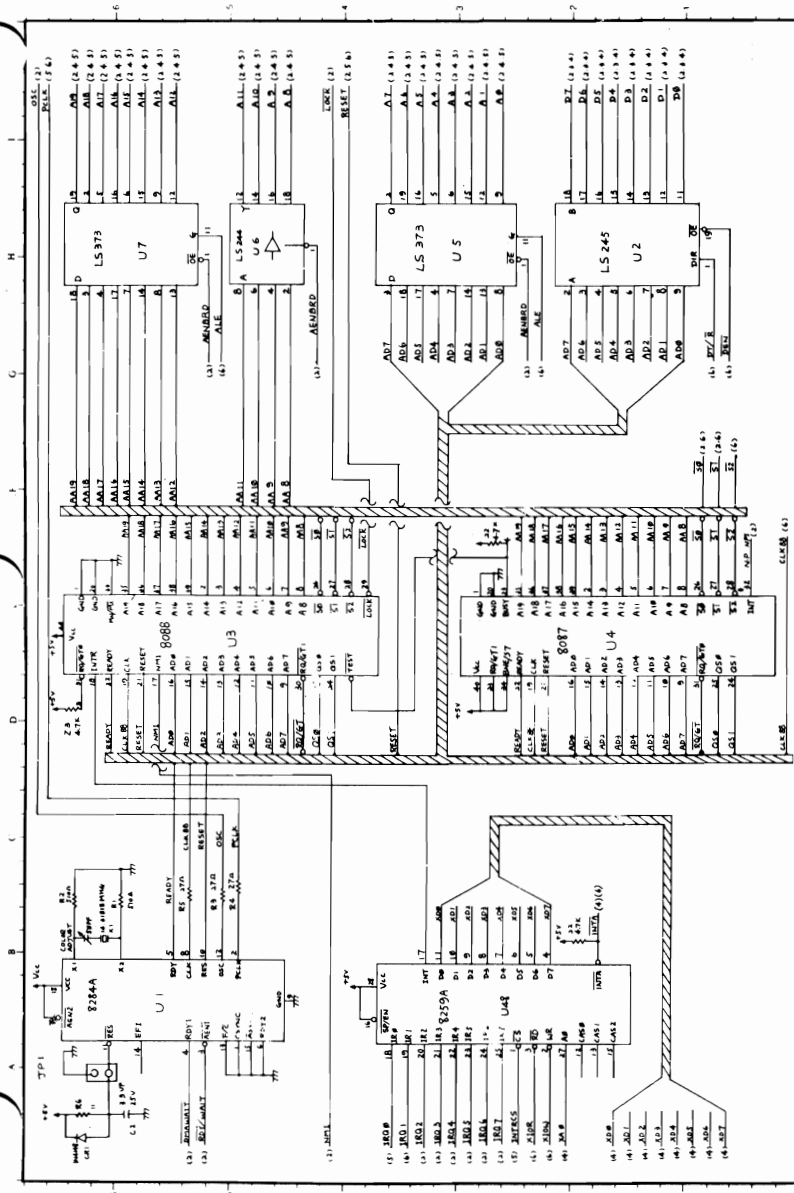
The keylock connector is a 2-pin, keyed, Berg strip. The pin assignments follow:



JP8

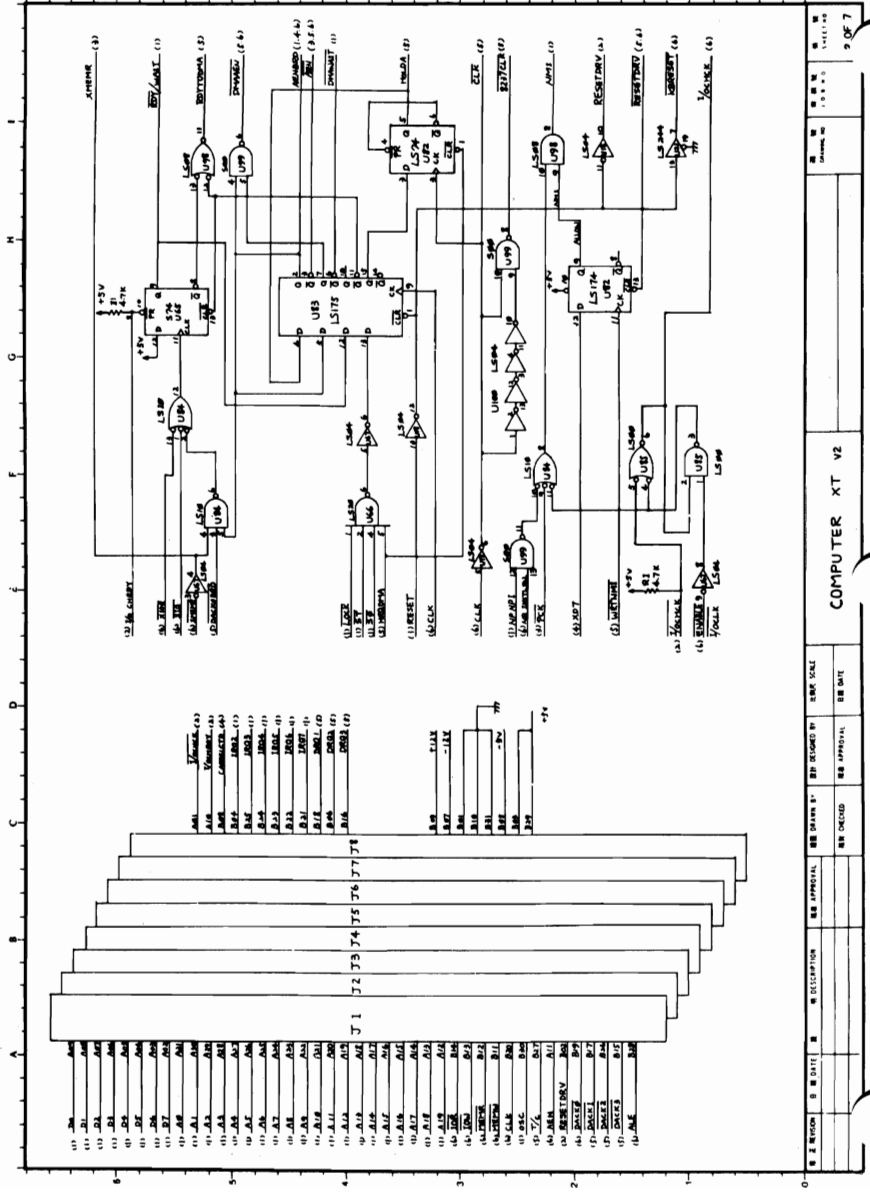
Keyboard locked, JP8 is open
Keyboard unlocked, JP8 is shortted



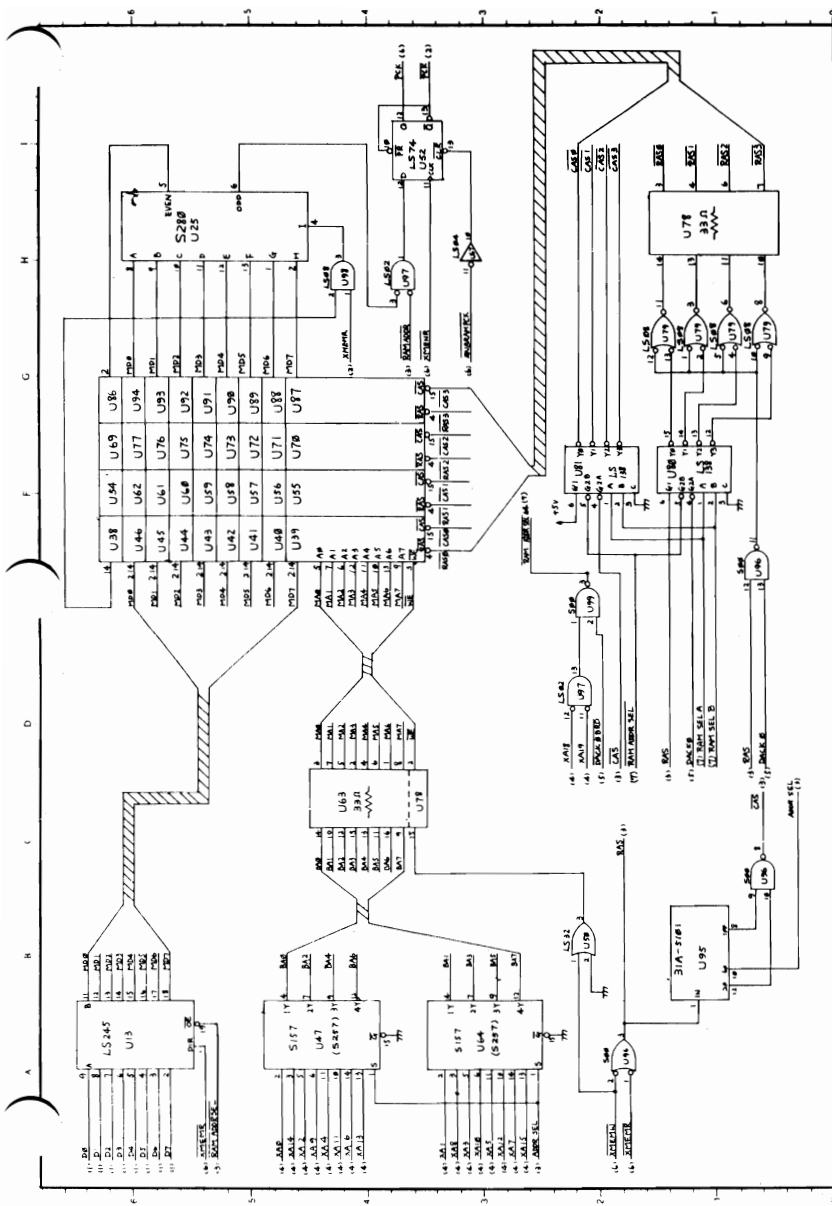


REV. (1,2)	REV. (3,4)	REV. (5,6)	REV. (7,8)	REV. (9,10)	REV. (11,12)	REV. (13,14)	REV. (15,16)	REV. (17,18)	REV. (19,20)	REV. (21,22)	REV. (23,24)	REV. (25,26)	REV. (27,28)	REV. (29,30)	REV. (31,32)	REV. (33,34)	REV. (35,36)	REV. (37,38)	REV. (39,40)	REV. (41,42)	REV. (43,44)	REV. (45,46)	REV. (47,48)	REV. (49,50)	REV. (51,52)	REV. (53,54)	REV. (55,56)	REV. (57,58)	REV. (59,60)	REV. (61,62)	REV. (63,64)	REV. (65,66)	REV. (67,68)	REV. (69,70)	REV. (71,72)	REV. (73,74)	REV. (75,76)	REV. (77,78)	REV. (79,80)	REV. (81,82)	REV. (83,84)	REV. (85,86)	REV. (87,88)	REV. (89,90)	REV. (91,92)	REV. (93,94)	REV. (95,96)	REV. (97,98)	REV. (99,100)																																																		
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COMPUTER XT V2

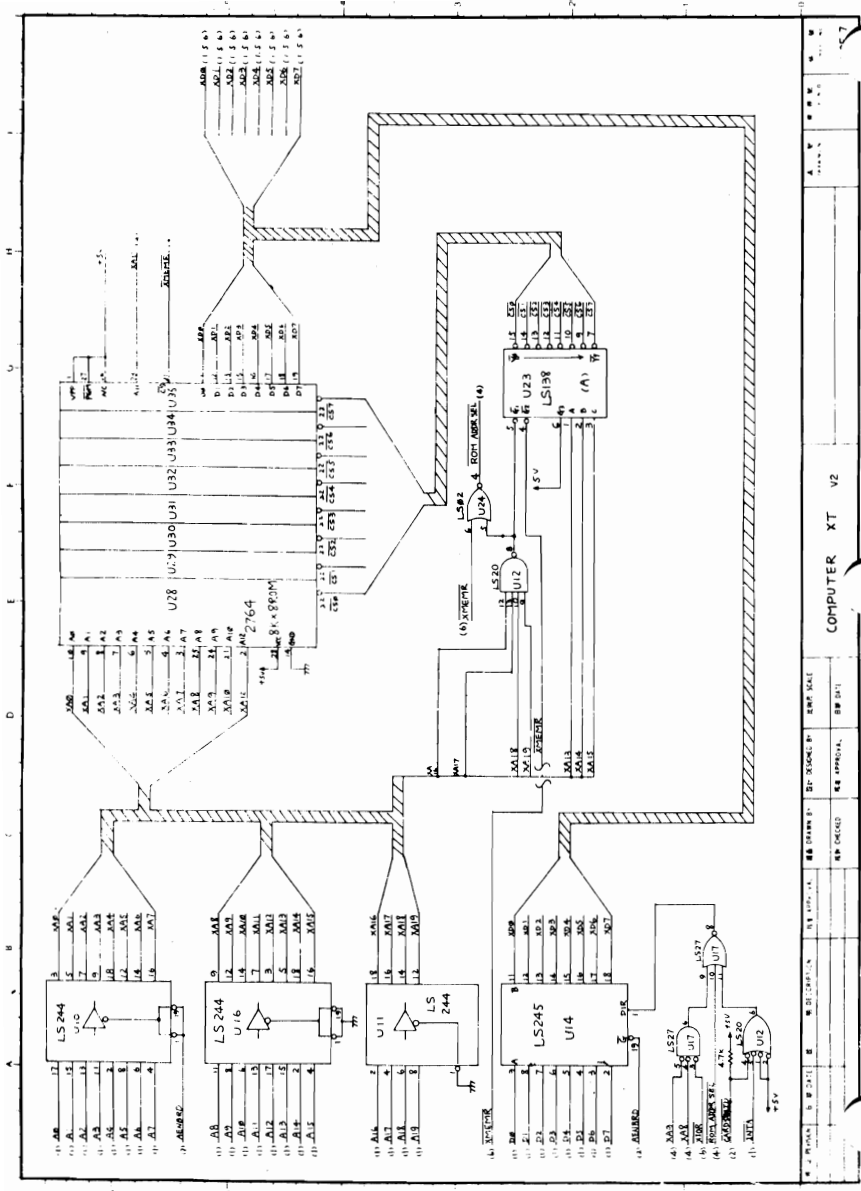


COMPUTER XT V2		REV. 11/11/74
COMPUTER XT V2		9 OF 7
DESIGN	CHECKED	APPROVAL
DATE	DATE	DATE
NAME OCCUPATION NAME APPROVAL NAME CHECKED NAME DATE		

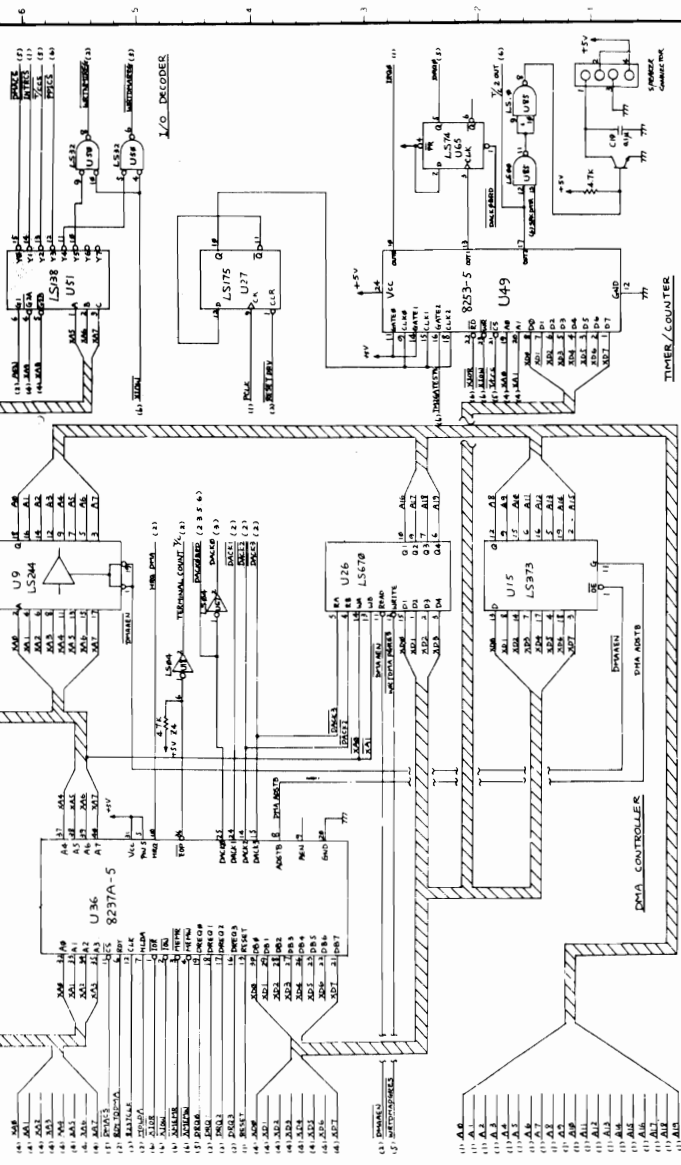


REV. 2	REVISION	BY	DATE	W. BUCKLEY, N.	REV. APPROVAL	DATE	3 OF 7
REV. 1	REVISION	BY	DATE	W. BUCKLEY, N.	REV. APPROVAL	DATE	3 OF 7
REV. 0	REVISION	BY	DATE	W. BUCKLEY, N.	REV. APPROVAL	DATE	3 OF 7

COMPUTER XT V2



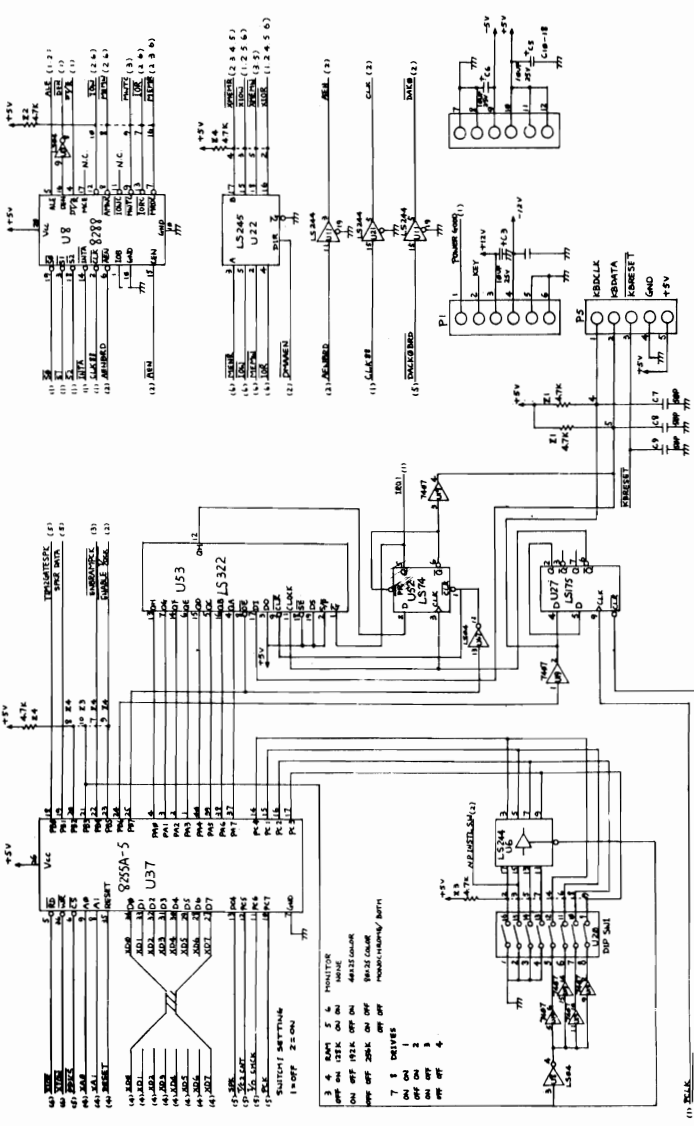
PROJECT	DATE	BY	REVISION	BY	DATE	DESCRIPTION
COMPUTER XT V2						



- (1) DATA BUS
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- (117) CONTROL BUS
- (118) DATA BUS
- (119) ADDRESS BUS
- (120) CONTROL BUS

A B C D E F G H

1 2 3 4 5 6



- (1) WALK
(2) HEAD
(3) SELECT
(4) DATA
(5) ADDRESS
(6) STROBE
(7) READY
(8) DATA
(9) ADDRESS
(10) STROBE
(11) READY
- U1: 74LS244 (1 2 3 4 5 6 7 8 9 10 11 12)
U2: 74LS244 (1 2 3 4 5 6 7 8 9 10 11 12)
U3: 6825A-5 (1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40)
U4: 74LS246 (1 2 3 4 5 6 7 8 9 10 11 12)
U5: 74LS123 (1 2 3 4 5 6 7 8 9 10 11 12)
U6: 74LS123 (1 2 3 4 5 6 7 8 9 10 11 12)

Pin headers: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40

Pin headers: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40

Pin headers: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40

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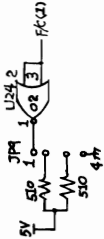
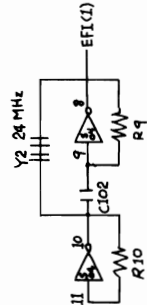
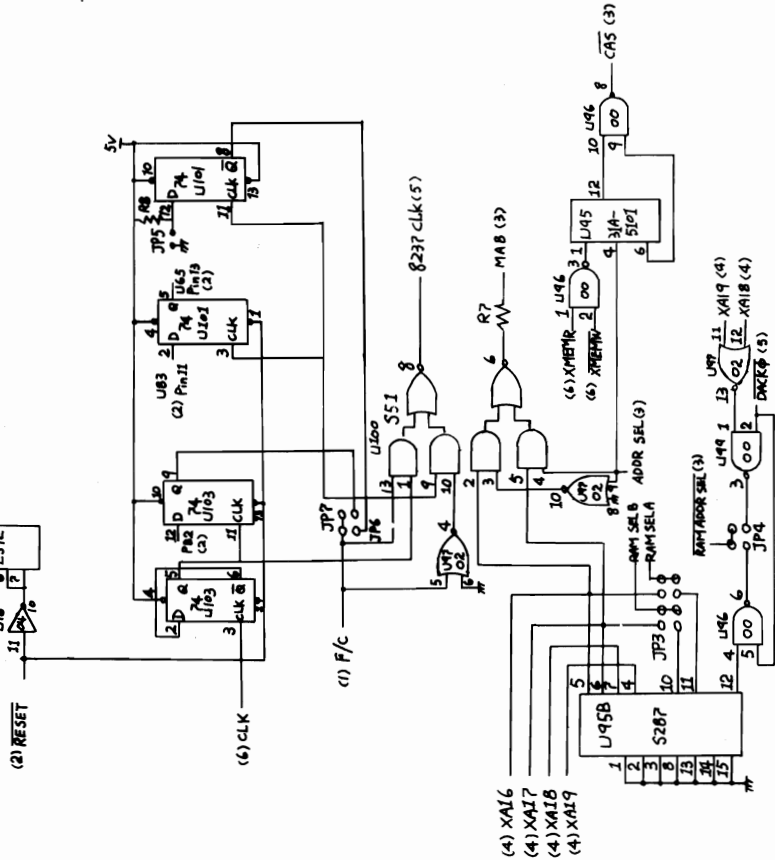
COMPUTER XT V2

(1) OSC 8 — 300pF — U102 — 8253 CLK (5)

(2) RESET

U106 6 LST2

U102 14



JPB PB7 (6)
 OE (6)

(4) XA16
 (4) XA17
 (4) XA18
 (4) XA19

